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(54) FLAT PANEL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

(76) Inventor: **Keum-Nam Kim**, Seoul-city (KR)

Correspondence Address:
STAAS & HALSEY LLP
700 11TH STREET, NW
SUITE 500
WASHINGTON, DC 20001 (US)

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(52) **U.S. Cl.** **349/43**; 349/138

(57) **ABSTRACT**

A flat panel display includes a pixel electrode having an opening portion formed on an insulating substrate, a semiconductor layer formed over a surface of the insulating substrate, spaced apart from the pixel electrode, having source and drain regions formed to both end portions thereof, a first insulating layer formed over the surface of the insulating substrate excluding the opening portion of the pixel electrode, a gate electrode formed on the first insulating layer over the semiconductor layer, and a second insulating layer formed over the surface of the insulating substrate excluding the opening portion of the pixel electrode. The present invention provides an organic EL display manufactured with reduced mask processes which has excellent electrical characteristics and improved light transmittance.

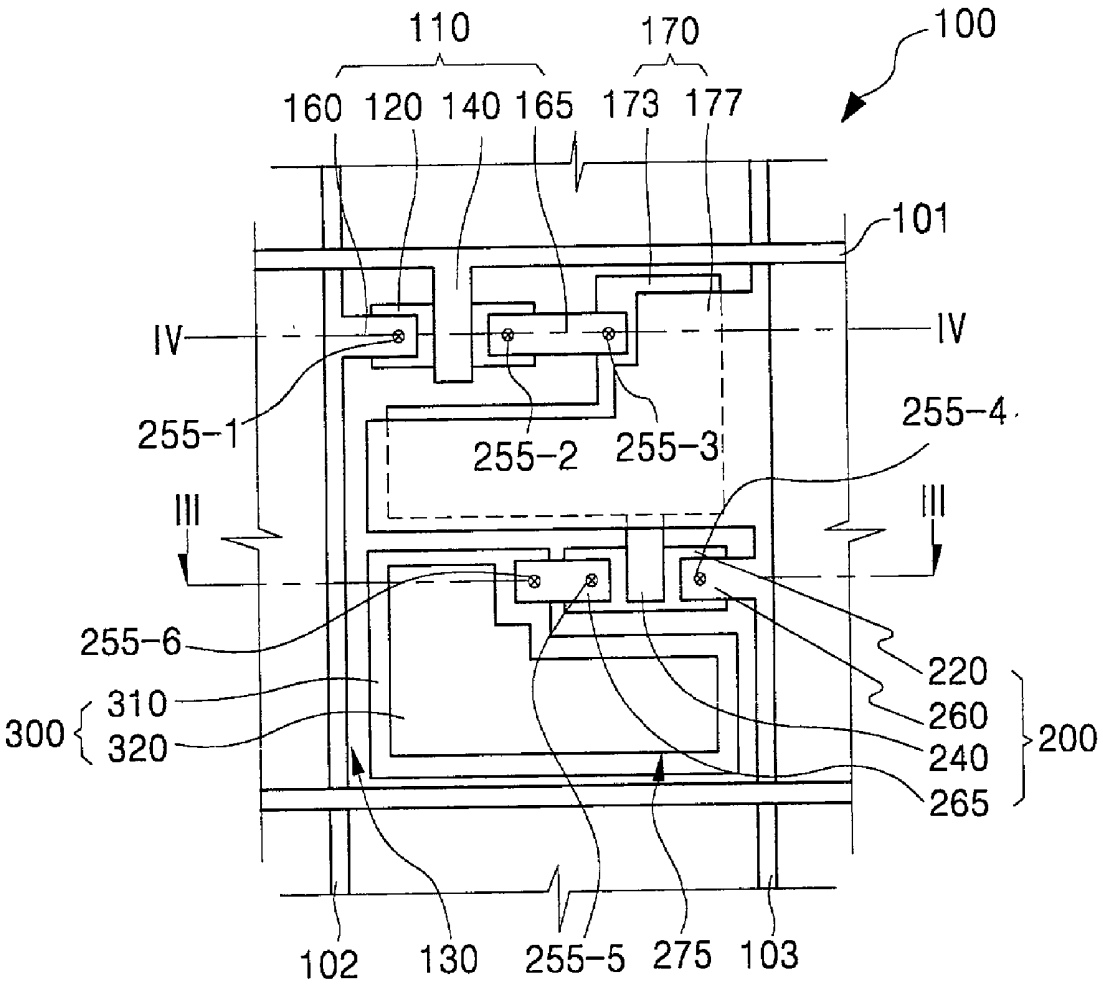


FIG. 1
(PRIOR ART)

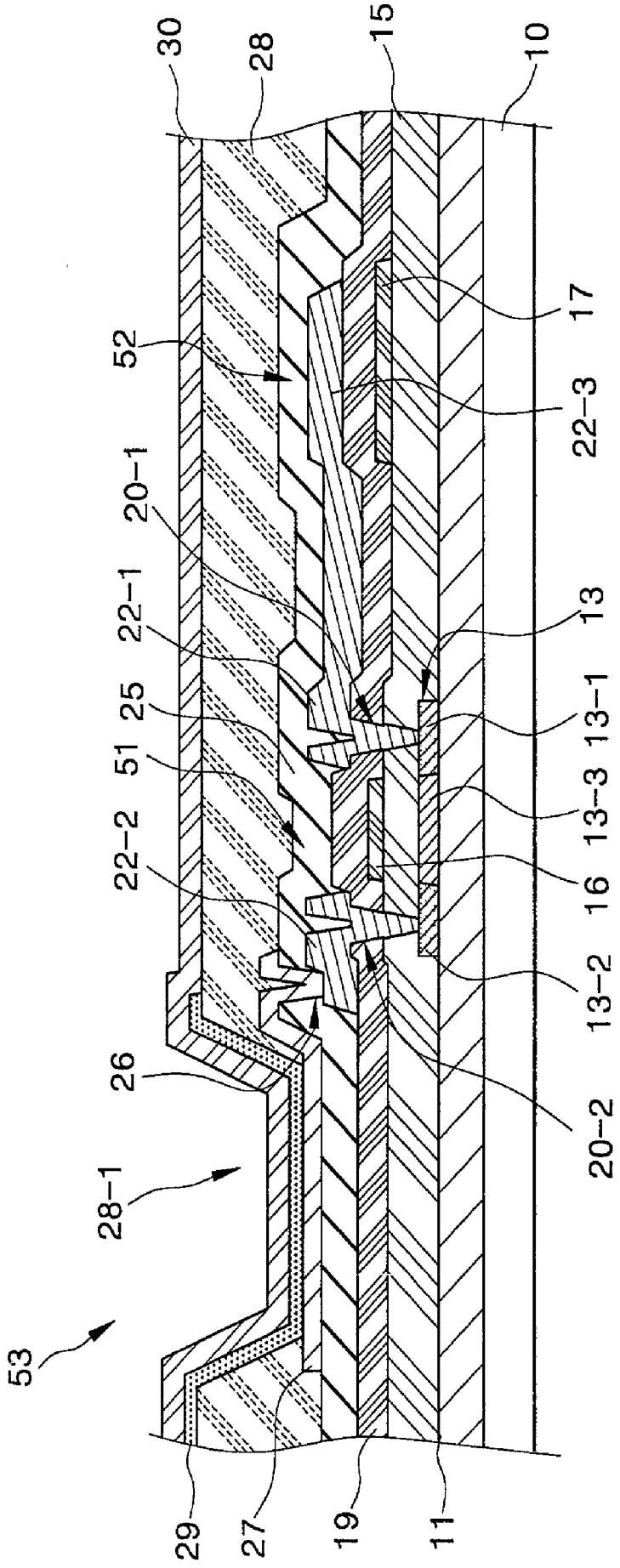


FIG. 2

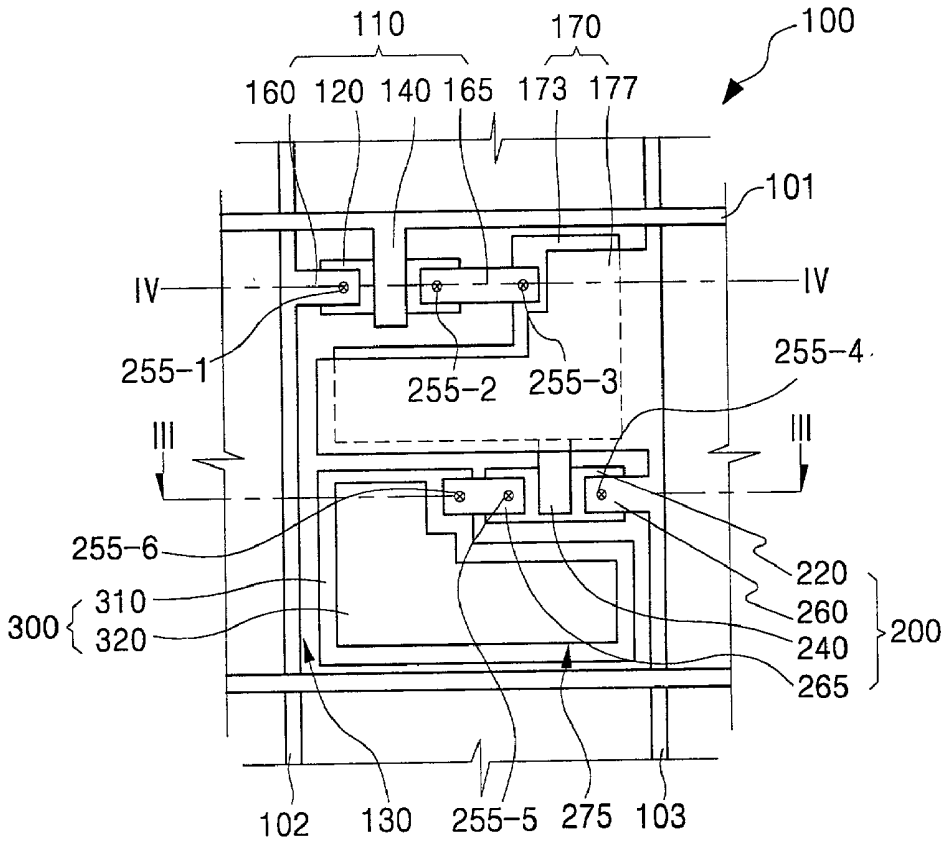


FIG. 3A

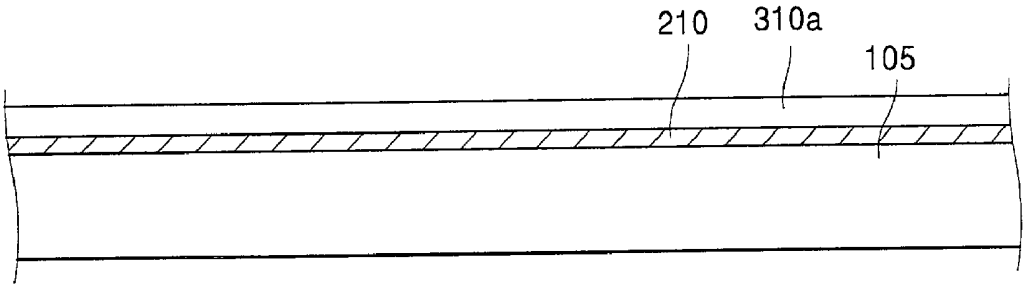


FIG. 3B

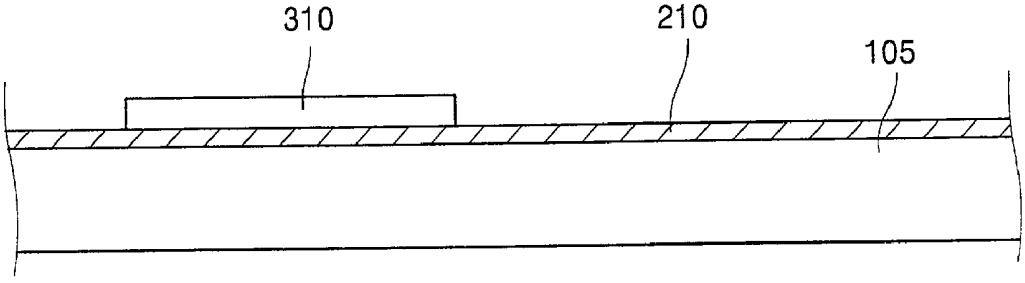


FIG. 3C

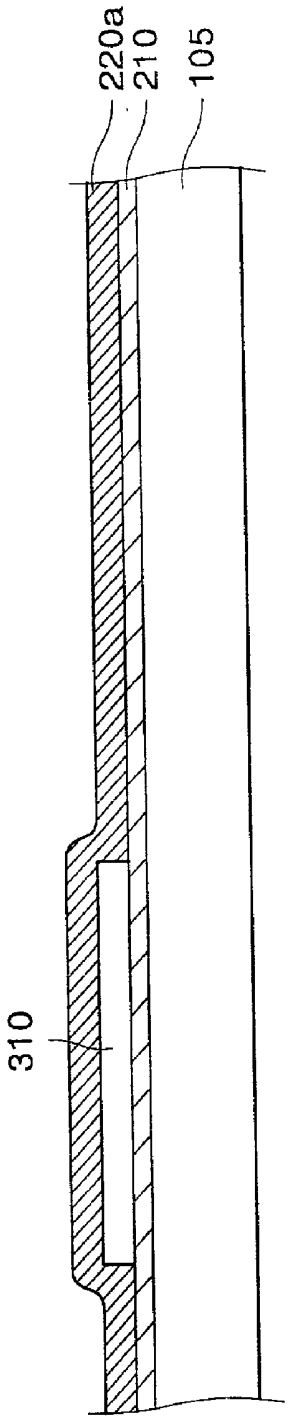


FIG. 3D

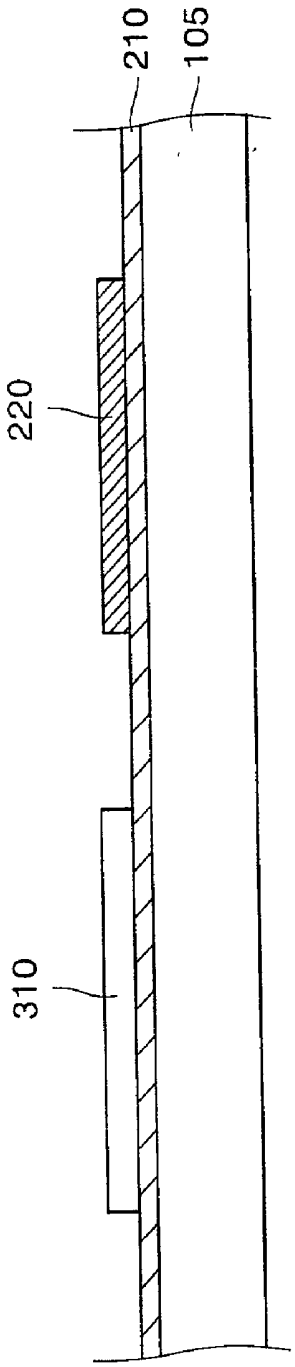


FIG. 3E

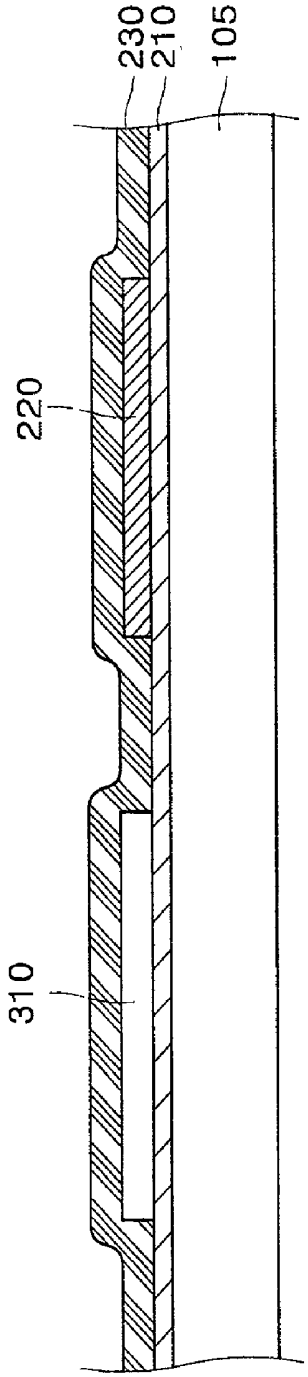


FIG. 3F

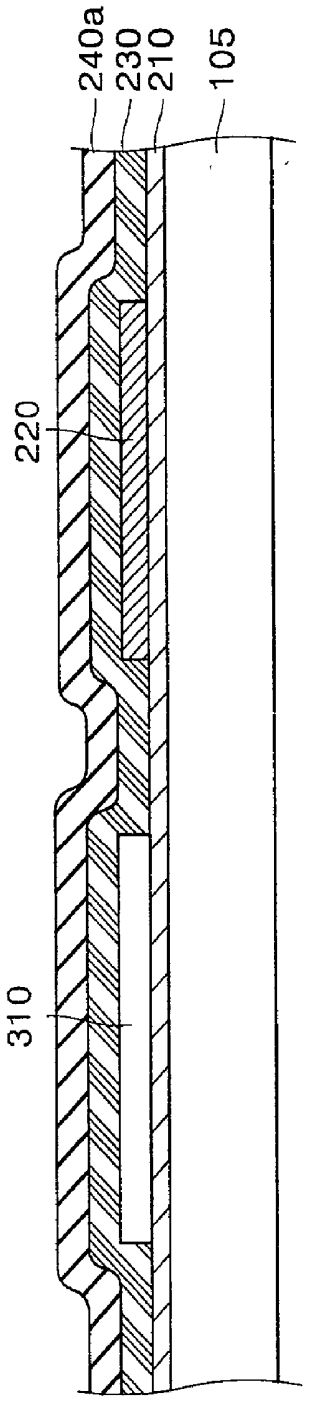


FIG. 3G

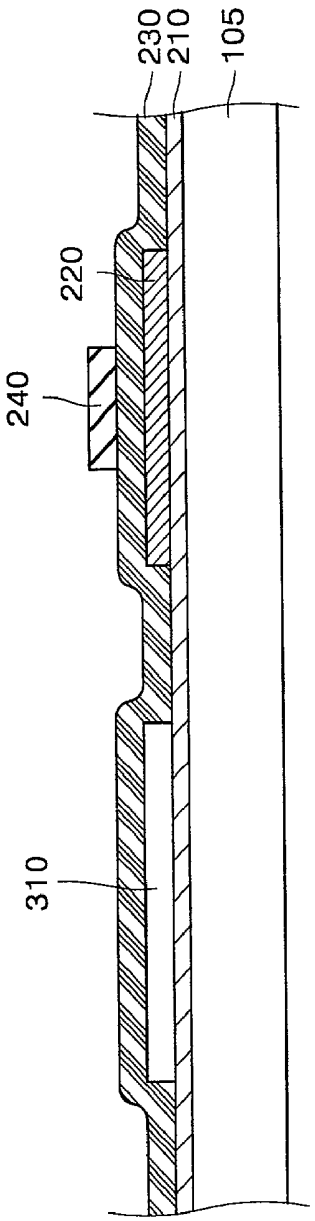

230
210
105
220
240
310

FIG. 3H

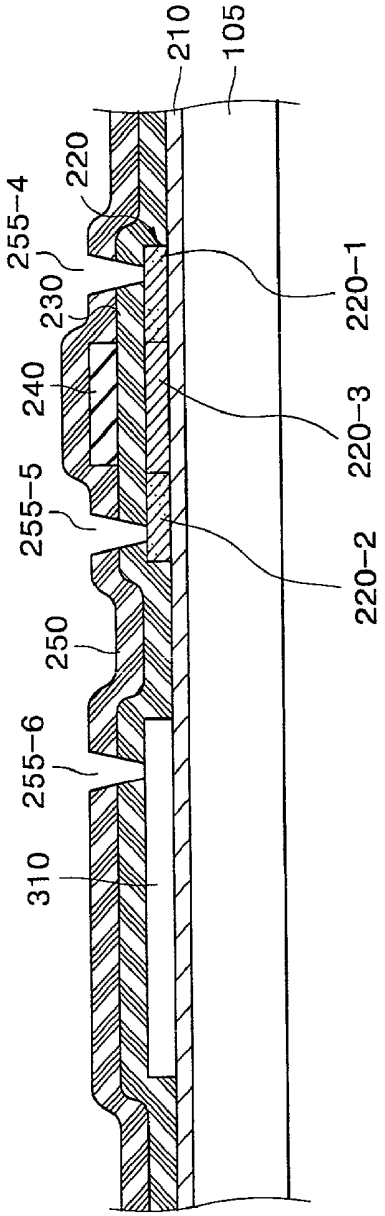

210
105
220
255-4
230
240
255-5
250
255-6
310
220-1
220-3
220-2

FIG. 3I

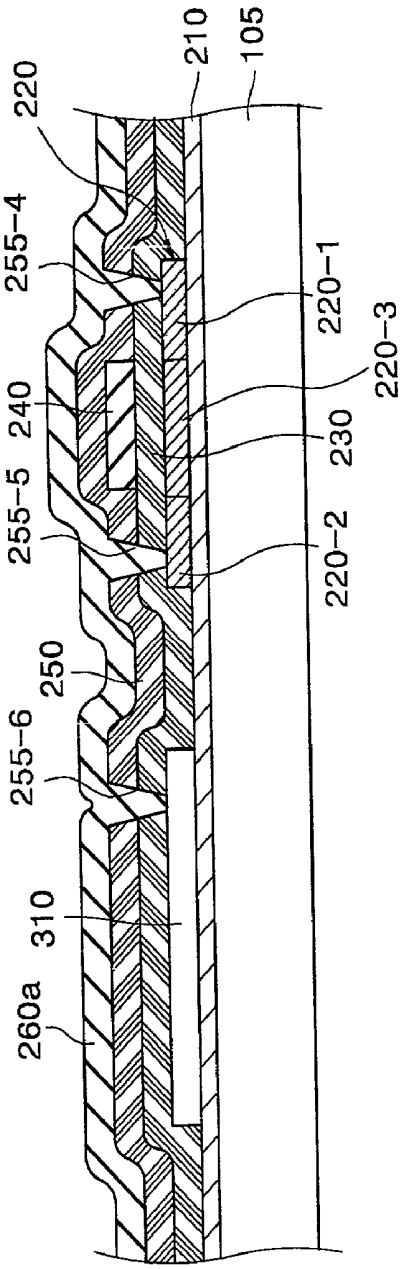

220
210
105
255-4
220-1
220-3
240
230
255-5
220-2
250
255-6
310
260a

FIG. 3J

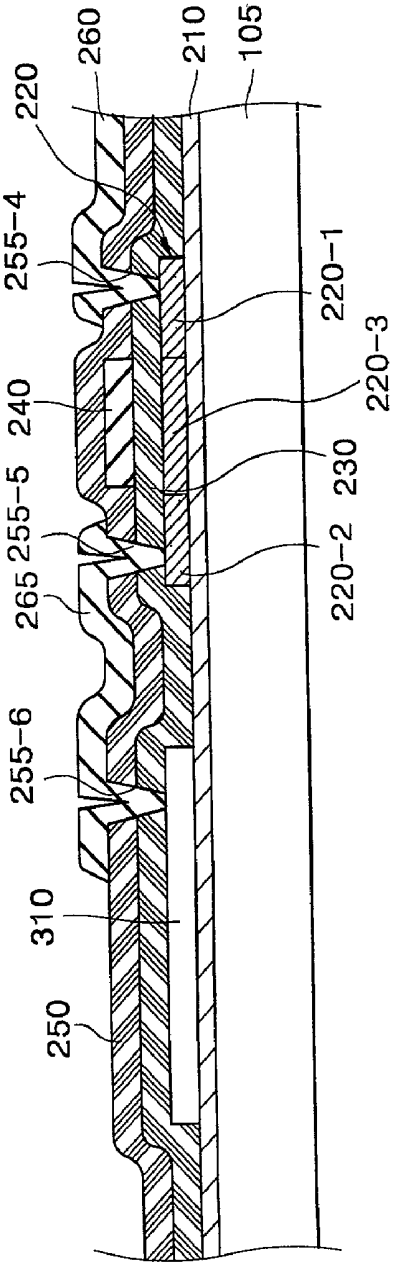

220
260
210
105
255-4
220-1
220-3
240
230
255-5
220-2
265
255-6
310
250

FIG. 3K

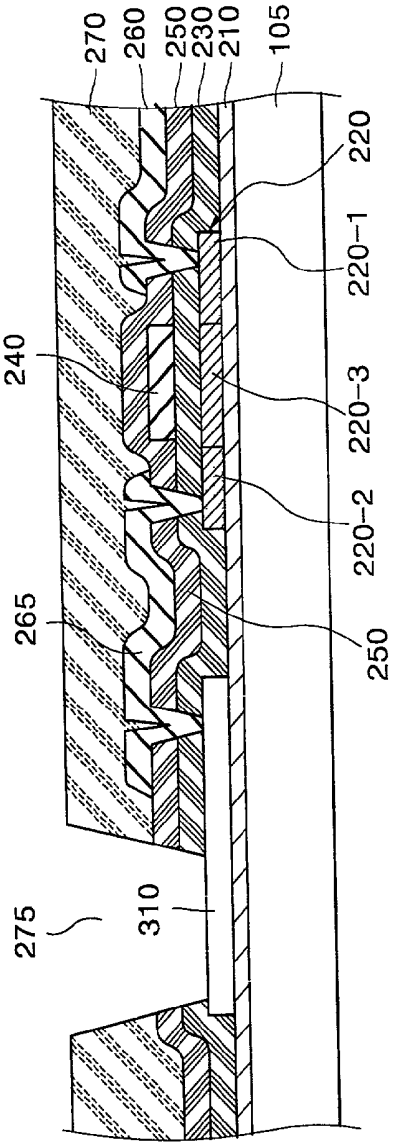

270
260
250
230
210
105
220
220-1
220-3
220-2
240
265
250
275
310

FIG. 3L

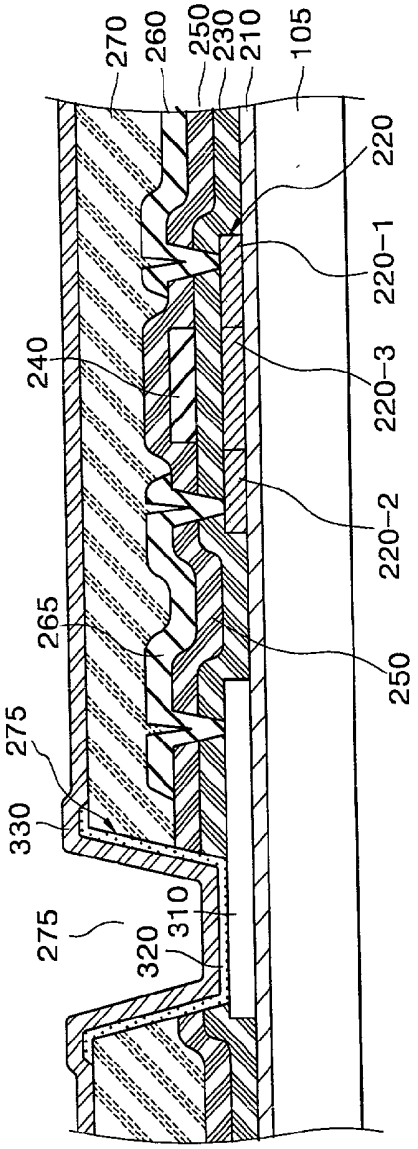
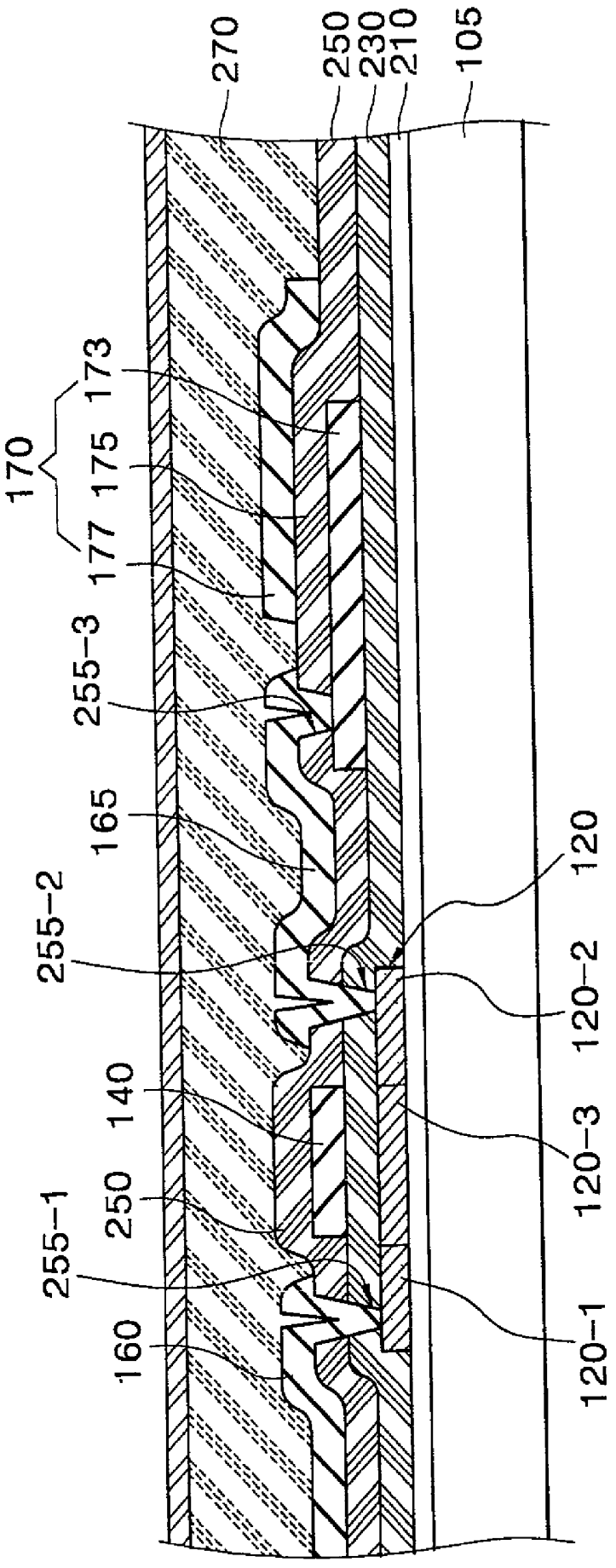

270
260
250
230
210
105
220
220-1
220-3
220-2
240
265
250
275
330
310
320

FIG. 4


270
250
230
210
105
173
170
175
177
255-3
165
255-2
120
120-2
140
120-3
250
255-1
160
120-1

FLAT PANEL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of Korean Patent Application No. 2001-19915, filed on Apr. 13, 2001, in the Korean Industrial Property Office, the disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a flat panel display and a method of manufacturing the same. More particularly, the present invention relates to an organic electroluminescence (EL) display and a method of manufacturing the same.

[0004] 2. Description of the Related Art

[0005] Electroluminescence (EL) displays have recently attracted considerable attention as a flat panel display. The EL displays generally use a thin film transistor (TFT) as a switching element.

[0006] **FIG. 1** is a cross-sectional view illustrating a conventional EL display. The conventional EL display of **FIG. 1** is manufactured as follows. First, a first insulating layer **11** is formed on the whole surface of a transparent insulating substrate **10**. The first insulating layer **11** serves as a buffer layer. The transparent insulating substrate **10** is made of a glass or a synthetic resin. A polysilicon layer is deposited on the buffer layer **11** and patterned into a semiconductor layer **13** using a first mask.

[0007] A second insulating layer **15** is formed over the whole surface of the transparent insulating substrate **10** and covers the semiconductor layer **13**. The second insulating layer **15** serves as a gate insulating layer.

[0008] A first metal layer is deposited on the first insulating layer **15** and patterned into a gate electrode **16** and a first capacitor electrode **17** using a second mask.

[0009] An n-type or a p-type impurity is ion-doped into the semiconductor layer **13** to form source and drain regions **13-1** and **13-2**. A portion **13-3** of the semiconductor layer **13** under the gate electrode **16** serves as an active area.

[0010] A third insulating layer **19** is formed over the whole surface of the transparent insulating substrate **10** and covers the gate electrode **16** and the first capacitor electrode **17**. The insulating layer **19** serves as an inter-insulating layer.

[0011] Subsequently, the second and third insulating layers **15** and **19** are etched using a third mask to form first and second contact holes **20-1** and **20-2**. The first contact hole **20-1** exposes a portion of the source region **13-1**, and the second contact hole **20-2** exposes a portion of the drain region **13-2**.

[0012] A second metal layer is deposited over the whole surface of substrate and patterned into source and drain electrodes **22-1** and **22-2** and a second capacitor electrode **22-3** using a fourth mask. The source electrode **22-1** contacts the source region **13-1** through the first contact hole **20-1**, and the drain electrode **22-2** contacts the drain region **13-2** through the second contact hole **20-2**. The second capacitor electrode **22-3** extends from either of the source and drain electrodes **22-1** and **22-2**, for example the source electrode **22-1**. Consequently, a TFT **51** and a capacitor **52** of the conventional EL display are completed.

[0013] At this point, a portion of the third insulating layer **19** between the first and second capacitor electrodes **17** and **22-3** serves as a dielectric layer of the capacitor **52**.

[0014] Thereafter, a fourth insulating layer **25** is formed over the whole surface of the transparent insulating substrate **10**. The fourth insulating layer **25** serves as a passivation layer. The passivation layer **25** is etched to form a via hole **26** at a region corresponding a portion of either of the source and drain electrodes **22-1** and **22-2** using a fifth mask. In **FIG. 1**, the via hole **26** exposes a portion of the drain electrode **22-2**.

[0015] A transparent material layer is deposited on the passivation layer **25** and patterned into a pixel electrode **27** using a sixth mask. The pixel electrode **27** is made of a transparent conductive material such as indium tin oxide (ITO) or indium zinc oxide (IZO). The pixel electrode **27** electrically contacts the drain electrode **22-2** through the via hole **26**. The pixel electrode **27** is used as an anode electrode.

[0016] A fifth insulating layer **28** is formed over the whole surface of the transparent insulating substrate **10**. The fifth insulating layer **28** serves as a planarization layer. The planarization layer **28** is etched using a seventh mask to form an opening portion **28-1**. The opening portion **28-1** exposes a portion of the anode electrode **27**.

[0017] An organic EL layer **29** is formed on the exposed portion of the anode electrode **27** and the planarization layer **28**. A third metal layer, i.e., a cathode electrode **30** is deposited to cover the whole display area, completing the conventional organic EL display **53**.

[0018] However, the conventional organic EL display has the following disadvantages. Since seven complicated mask processes are used to manufacture the organic EL display, production cost is high and manufacturing yield is low. Also, during an etching process to form the anode electrode **27**, an etching solution can soak into the source and drain electrodes **22-1** and **22-2**, whereupon the source and drain electrodes **22-1** and **22-2** can be damaged, thereby deteriorating electrical characteristics of the TFT. Furthermore, light emitted from the organic EL layer **29** is reflected from an interface between the gate insulating layer **15** and the inter-insulating layer **19**, and an interface between the inter-insulating layer **19** and the passivation layer **25**, thereby lowering a light transmittance.

SUMMARY OF THE INVENTION

[0019] To overcome the problems described above, embodiments of the present invention provide an organic EL display having a high manufacturing yield by reducing mask processes.

[0020] It is another object of the present invention to provide an organic EL display having excellent electrical characteristics.

[0021] It is a still another object of the present invention to provide an organic EL display having a high light transmittance.

[0022] Additional objects and advantages of the invention will be set forth in part in the description which follows and, in part, will be obvious from the description, or may be learned by practice of the invention.

[0023] To achieve the above and other objects of the present invention, there is provided a flat panel display, comprising a pixel electrode having an opening portion formed on an insulating substrate, a semiconductor layer formed over a surface of the insulating substrate that is spaced apart from the pixel electrode having source and drain regions formed at both end portions of the semiconductor, a first insulating layer formed over the surface of the insulating substrate excluding the opening portion of the pixel electrode, a gate electrode formed on the first insulating layer over the semiconductor layer, and a second insulating layer formed over the surface of the insulating substrate excluding the opening portion of the pixel electrode.

[0024] The flat panel display, further comprising contact holes formed in the first and second insulating layers which expose a portion of the pixel electrode and portions of the source and drain regions of the semiconductor layer, source and drain electrodes formed on the second insulating layer, wherein the source electrode is electrically connected to the source region through one of the contact holes, and the drain electrode is electrically connected to the drain region and the pixel electrode through the other of the contact holes, and a third insulating layer formed over the surface of the insulating substrate excluding the opening portion of the pixel electrode.

[0025] The opening portion has an area size smaller than the pixel electrode. The third insulating layer is a planarization layer that is made of SiN_x, SiO_x, acryl or a photoresist layer.

[0026] The present invention provides a method of manufacturing a flat panel display, comprising forming a pixel electrode and a semiconductor layer, spaced apart from each other, on an insulating substrate, forming a first insulating layer over a surface of the insulating substrate to cover the pixel electrode and the semiconductor layer, forming a gate electrode on a portion of the first insulating layer corresponding to a location of the semiconductor layer, forming a second insulating layer over the surface of the insulating substrate to cover the gate electrode, forming contact holes in the first and second insulating layers to expose a portion of the pixel electrode and portions of the semiconductor layer, forming source and drain electrodes on the second insulating layer electrically connecting the source electrode to the semiconductor layer through one of the contact holes and electrically connecting the drain electrode to the semiconductor layer and the pixel electrode through the other of the contact holes, forming a photoresist layer over the surface of the insulating substrate exposing a portion of the second insulating layer over the pixel electrode, and forming an opening portion by etching the first and second insulating layers using the photoresist layer as a mask.

[0027] When the semiconductor layer and the pixel electrode are formed on the insulating substrate, the pixel electrode is formed after the semiconductor layer. Otherwise, the pixel electrode is formed before the semiconductor layer.

[0028] The method further comprising forming a third insulating layer over the surface of the insulating substrate before forming the photoresist layer and removing the remaining photoresist layer after forming the opening portion using the photoresist layer as a mask.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] These and other objects and advantages of the present invention will become more apparent and more readily appreciated from the following description of the preferred embodiments, taken in conjunction with the accompanying drawings of which:

[0030] **FIG. 1** is a diagram illustrating a cross-sectional view of a conventional EL display;

[0031] **FIG. 2** is a diagram illustrating a plan view of an organic EL display according to an embodiment of the present invention;

[0032] **FIGS. 3A** to **3**L are diagrams of cross-sectional views taken along line III-III of **FIG. 2** illustrating a method of manufacturing a flat panel display according to an embodiment of the present invention; and

[0033] **FIG. 4** is a diagram illustrating a cross-sectional view of the flat panel display taken along line IV-IV of **FIG. 2**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0034] Reference will now be made in detail to preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The embodiments are described below in order to explain the present invention by referring to the figures.

[0035] **FIG. 2** shows a plan view illustrating an organic EL display **100** according to an embodiment of the present invention. Referring to **FIG. 2**, the organic EL display **100** includes pixels **130**, where each pixel **130** includes first and second TFTs **110** and **200**, a storage capacitor **170**, and an organic EL element **300**.

[0036] The pixel **130** is formed at a region defined by two adjacent gate lines **101**, a data line **102** and a power supplying line **103**. The gate lines **101** are arranged in a transverse direction. The data line **102** and the power supplying line **103** are arranged in a perpendicular direction to the gate lines **101**. The gate lines **101** serve to apply a thin film transistor (TFT) on/off current. The data line **102** serves to apply a data voltage. The power supplying line **103** serves to supply a current for driving the organic EL display **100**.

[0037] The first TFT **110** is arranged at a location adjacent to a crossing point of the gate lines **101** and the data line **102**. The first TFT **110** includes a semiconductor layer **120**, a gate electrode **140**, and source and drain electrodes **160** and **165**. The semiconductor layer **120** includes source and drain regions **120-1** and **120-2** and an active area **120-3** (see **FIG. 4**). The gate electrode **140** extends from the gate line **101**. The source electrode **160** extends from the data line **102**, and is electrically connected to the source region **120-1** of the semiconductor layer **120** through a first contact hole **255-1**. The drain electrode **165** is electrically connected to the drain region **120-2** through a second contact hole **255-2**.

[0038] The storage capacitor **170** serves to store a data voltage required to drive the second TFT **200** during one

frame. The storage capacitor **170** includes first and second capacitor electrodes **173** and **177** with a dielectric layer **175** interposed therebetween (see **FIG. 4**). The first capacitor electrode **173** is electrically connected to the drain electrode **165** of the first TFT **110** through a third contact hole **255-3**. The second capacitor electrode **177** extends from the power supplying line **103**.

[**0039**] The second TFT **200** includes a semiconductor layer **220**, a gate electrode **240**, and source and drain electrodes **260** and **265**. The semiconductor layer **220** includes source and drain regions **220-1** and **220-2** and an active area **220-3** (see **FIG. 3L**). The gate electrode **240** extends from the first capacitor electrode **173**. The source electrode **260** extends from the power supplying line **103** and is electrically connected to the source region **220-1** of the semiconductor layer **220** through a fourth contact hole **255-4**. The drain electrode **265** serves to apply a driving voltage to the organic EL element **300** and is electrically connected to the drain region **220-2** of the semiconductor layer **220** through a fifth contact hole **255-5**.

[**0040**] The organic EL element **300** includes an anode electrode **310** and a cathode electrode **330** with an organic EL layer **320** (see **FIG. 3L**) interposed therebetween. The anode electrode **310** is electrically connected to the drain electrode **265** of the second TFT **200** through a sixth contact hole **255-6**. An opening portion **275** is formed on the anode electrode **310**, and the organic EL layer **320** is formed on the anode electrode **310** to cover the opening portion **275**.

[**0041**] Hereinafter, a process of manufacturing the organic EL display of **FIG. 2** is described with reference to **FIGS. 3A** to **3L** and **4**. **FIGS. 3A** to **3L** show cross-sectional views taken along line III -III of **FIG. 2**. **FIG. 4** shows a cross-sectional view taken along line IV-IV of **FIG. 2**.

[**0042**] **FIG. 3A** shows that a first insulating layer **210** is formed on the whole surface of a transparent insulating substrate ("substrate") **105** as a buffer layer. The buffer layer **210** serves to prevent an influx of an impurity. A transparent conductive material layer **310***a* is deposited on the buffer layer **210**.

[**0043**] **FIG. 3B** shows that the transparent conductive material layer **310***a* is patterned into an anode electrode, i.e., a pixel electrode **310** using a first mask.

[**0044**] **FIG. 3C** shows that a polysilicon layer **220***a* is deposited over the whole surface of the substrate **105** to cover the anode electrode **310**. At this point, according to an embodiment of the invention, the polysilicon layer **220***a* is formed such that an amorphous silicon layer is deposited and then annealed. However, the amorphous silicon layer need not be deposited in all circumstances.

[**0045**] Referring to **FIGS. 3D and 4**, the polysilicon layer **220***a* is patterned using a second mask to form the semiconductor layers **120** and **220**. In this embodiment, when the pixel electrode **310** and the semiconductor layers **120** and **220** are formed on the substrate **105**, the pixel electrode **310** is formed and then the semiconductor layers **120** and **220** are formed. Otherwise, the semiconductor layers **120** and **220** are formed and then the pixel electrode **310** is formed.

[**0046**] Subsequently, **FIGS. 3E and 4** show that a second insulating layer **230** is formed over the whole surface of the substrate **105** and covers the semiconductor layers **120** and **220**. The second insulating layer **230** serves as a gate insulating layer.

[**0047**] **FIGS. 3F and 4** show that a first metal layer **240***a* is deposited on the second insulating layer **230**. **FIGS. 3G and 4** show that the first metal layer **240***a* is patterned into the gate electrodes **140** and **240** and the first capacitor electrode **173** using a third mask.

[**0048**] **FIGS. 3H and 4** show that an n-type or a p-type impurity is ion-doped into the semiconductor layers **120** and **220** to form the source and drain regions **120-1** and **120-2**, and **220-1** and **220-2**, respectively. Portions **120-3** and **220-3** of the semiconductor layers **120** and **220** under the gate electrodes **140** and **240** serve as an active area, respectively.

[**0049**] A third insulating layer **250** is formed over the whole surface of the substrate **105** and covers the gate electrodes **140** and **240**. The third insulating layer **250** serves as an inter-insulating layer. A portion of the inter-insulating layer **250** corresponding to the first capacitor electrode **173** serves as the dielectric layer **175** of the storage capacitor **170**. The gate insulating layer **230** and the inter-insulating layer **250** are etched using a fourth mask to form first to sixth contact holes, **255-1** to **255-6**.

[**0050**] Thereafter, **FIGS. 31 and 4** show that a second metal layer **260***a* is deposited on the inter-insulating layer **250**.

[**0051**] **FIGS. 3J and 4** show that the second metal layer **260***a* is patterned using a fifth mask to form the source and drain electrodes **160** and **165** of the first TFT **110**, the source and drain electrodes **260** and **265** of the second TFT **200** and the second capacitor electrode **177**.

[**0052**] The source electrode **160** is electrically connected to the source region **120-1** through the first contact hole **255-1**. One end of the drain electrode **165** is electrically connected to the drain region **120-2** through the second contact hole **255-2**, and the other end is electrically connected to the first capacitor electrode **173** through the third contact hole **255-3**. The source electrode **260** is electrically connected to the source region **220-1** through the fourth contact hole **255-4**. One end of the drain electrode **265** is electrically connected to the drain region **220-2** through the fifth contact hole **255-5**, and the other end is electrically connected to the anode electrode **310** through the sixth contact hole **255-6**.

[**0053**] Subsequently, **FIGS. 3K and 4** show that a fourth insulating layer **270** is formed over the whole surface of the substrate **105** as a planarization layer. The planarization layer **270** is etched using a sixth mask to expose a portion of the anode electrode **310**, thereby forming an opening portion **275** on the anode electrode **310**. The opening portion **275** has an area size smaller than the anode electrode **310** so that the organic EL layer **330** is deposited not to be tangent to an edge portion of the anode electrode **310**. When the organic EL layer **330** is tangent to the edge portion of the anode electrode **310**, a strong electric field is generated at the edge portion of the anode electrode **310**, thereby shortening a life span of the organ EL display.

[**0054**] The first to third insulating layers are made of, for example, SiN_x or SiO_x, and the fourth insulating layer is made of, for example, SiN_x, SiO_x or acryl.

[0055] In this embodiment of the present invention, the opening portion **275** is formed according to the following method. First, the planarization layer **270** is formed on the inter-insulating layer **250**, and then a photoresist pattern is formed on the planarization layer **270**. The planarization layer **270** is made of SiN_x or SiO_x. The gate insulating layer **230**, the inter-insulating layer **250** and the planarization layer **270** are simultaneously etched according to the photoresist pattern to form the opening portion **275**. The remaining photoresist pattern is removed. Alternatively, the opening portion **275** can be formed such that a photoresist pattern is formed on the inter-insulating layer **250**, and then the gate insulating layer **230** and the inter-insulating layer **250** are simultaneously etched according to the photoresist pattern, wherein the photoresist pattern is used as the planarization layer. Since a process to form the passivation layer can be omitted or the photoresist pattern can substitute the planarization layer, the manufacturing process can be further simplified.

[0056] Subsequently, **FIGS. 3L and 4** show that the organic EL layer **320** is formed on the exposed portion of the anode electrode **310**. Finally, a third metal layer **330** is formed on the planarization layer **270** to cover the organic EL layer **320**. The third metal layer **330** is used as a cathode electrode.

[0057] Even though not shown, the organic EL layer **320** generally includes a hole transport layer, a luminescent layer, and an electron transport layer that are laminated in sequence and are sandwiched between the anode electrode and the cathode electrode.

[0058] The gate lines **101** (see **FIG. 2**) are formed at the same time as the gate electrodes **140** and **240**, and the data line **102** and the power supplying line **103** (see **FIG. 2**) are formed at the same time as the source and drain electrodes **160** and **165**, and **260** and **265**.

[0059] As described above, the organic EL display according to an embodiment of the present invention is manufactured using six mask processes compared to the conventional process that uses **7** mask processes. The reduction of the masking process in the present invention increases the overall manufacturing yield. Furthermore, since the insulating layers are not arranged at a region corresponding to the organic EL layer **320**, a light transmittance can be significantly improved. In addition, since the pixel electrode **310** is formed before a process to form the source and drain electrodes **260** and **265**, it is possible to prevent the source and drain electrodes from being damaged by an etch process (if the pixel electrode **310** is formed after the source and drain electrodes), thereby improving electric characteristics of the TFT.

[0060] The present invention is described with a focus on an organic EL display. However, the present invention can be applied to other flat panel displays such as a liquid crystal display (LCD).

[0061] Although a few embodiments of the present invention have been shown and described, it will be appreciated by those skilled in the art that changes may be made in these embodiments without departing from the principles and spirit of the invention, the scope of which is defined in the appended claims and their equivalents.

What is claimed is:

1. A flat panel display, comprising:

a substrate;

a pixel electrode having an opening portion formed on said substrate;

a semiconductor layer formed over a surface of said substrate that is spaced apart from said pixel electrode and having source and drain regions formed at both end portions thereof;

a first insulating layer formed over the surface of said substrate except over the opening portion of said pixel electrode;

a gate electrode formed on said first insulating layer over said semiconductor layer; and

a second insulating layer formed over the surface of said substrate except the opening portion of said pixel electrode.

2. The flat panel display of claim 1, further comprising:

contact holes formed in said first and second insulating layers, which expose a portion of said pixel electrode and portions of the source and drain regions of said semiconductor layer;

source and drain electrodes formed on said second insulating layer, wherein the source electrode is electrically connected to the source region through one of the contact holes, and the drain electrode is electrically connected to the drain region and said pixel electrode through another one of the contact holes; and

a third insulating layer formed over the surface of said substrate except the opening portion of said pixel electrode.

3. The flat panel display of claim 2, wherein the third insulating layer is a planarization layer comprising one of an oxide layer, a nitride layer, SiNx, SiOx, and acryl.

4. The flat panel display of claim 3, wherein the opening portion has an area sized to be smaller than an area of said pixel electrode.

5. The flat panel display of claim 2, wherein the third insulating layer is a planarization layer that is made of a photoresist layer.

6. The flat panel display of claim 1, wherein the opening portion has an area sized smaller than an area of said pixel electrode.

7. A method of manufacturing a flat panel display, comprising:

forming a pixel electrode and a semiconductor layer, spaced apart from each other, on a substrate;

forming a first insulating layer over a surface of the substrate to cover the pixel electrode and the semiconductor layer;

forming a gate electrode on a portion of the first insulating layer corresponding to a location of the semiconductor layer;

forming a second insulating layer over the surface of the substrate to cover the gate electrode;

forming contact holes in the first and second insulating layers to expose a portion of the pixel electrode and portions of the semiconductor layer;

forming source and drain electrodes on the second insulating layer electrically connecting the source electrode to the semiconductor layer through one of the contact holes, and electrically connecting the drain electrodes to the semiconductor layer and the pixel electrode through another one of the contact holes;

forming a photoresist layer over the surface of the substrate exposing a portion of the second insulating layer over the pixel electrode; and

forming an opening portion by etching the first and second insulating layers using the photoresist layer as a mask.

8. The method of claim 7, wherein said forming of the pixel electrode and the semiconductor layer comprises forming the pixel electrode after forming the semiconductor layer.

9. The method of claim 7, wherein said forming of the pixel electrode and the semiconductor layer comprises forming the pixel electrode before forming the semiconductor layer.

10. The method of claim 7, wherein said forming of the semiconductor layer comprises:

forming a polysilicon layer on the substrate; and

patterning the polysilicon layer to form the semiconductor layer.

11. The method of claim 7, wherein said forming of the semiconductor layer comprises:

depositing an amorphous silicon layer on the substrate;

annealing the amorphous silicon layer to form a polysilicon layer; and

patterning the polysilicon layer to form the semiconductor layer.

12. The method of claim 7, wherein said forming of the semiconductor layer comprises:

forming a polysilicon layer on the substrate; and

patterning the polysilicon layer to form the semiconductor layer.

13. The method of claim 12, wherein said forming of the gate electrode comprises:

depositing a first metal layer on the first insulating layer; and

patterning the first metal layer to form the gate electrode.

14. The method of claim 13, further comprising forming source and drain regions at corresponding end portions of the semiconductor layer.

15. The method of claim 14, wherein said forming of the source and drain electrodes comprises:

depositing a second metal layer on the second insulating layer; and

patterning the second metal layer to form the source and drain electrodes.

16. The method of claim 15, wherein said forming of the opening portion comprises using the remaining photoresist layer as a planarization layer.

17. The method of claim 16, wherein said forming of the pixel electrode and the semiconductor layer comprises forming the pixel electrode after forming the semiconductor layer.

18. The method of claim 16, wherein said forming of the pixel electrode and the semiconductor layer comprises forming the pixel electrode before forming the semiconductor layer.

19. The method of claim 15, further comprising:

forming a third insulating layer over the surface of the substrate before the forming of the photoresist layer; and

removing the remaining photoresist layer after the forming of the opening portion using the photoresist layer as a mask.

20. The method of claim 19, wherein the third insulating layer comprises one of an oxide layer, a nitride layer and an acryl layer.

21. The method of claim 7, wherein said forming of the opening portion comprises using the remaining photoresist layer as a planarization layer.

22. The method of claim 7, further comprising:

forming a third insulating layer over the surface of the substrate before the forming of the photoresist layer; and

removing the remaining photoresist layer after the forming of the opening portion using the photoresist layer as a mask.

* * * * *

专利名称(译)	平板显示装置及其制造方法		
公开(公告)号	US20020149710A1	公开(公告)日	2002-10-17
申请号	US10/038772	申请日	2002-01-08
[标]申请(专利权)人(译)	KIM KEUM NAM		
申请(专利权)人(译)	KIM KEUM-NAM		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	KIM KEUM NAM		
发明人	KIM, KEUM-NAM		
IPC分类号	H05B33/10 H01L21/77 H01L21/84 H01L27/12 H01L27/32 G02F1/1333		
CPC分类号	H01L27/1214 H01L27/3244 H01L27/1288 H01L27/3248 H01L51/56 H01L27/3246		
优先权	1020010019915 2001-04-13 KR		
其他公开文献	US6958252		
外部链接	Espacenet USPTO		

摘要(译)

一种平板显示器，包括：像素电极，具有形成在绝缘基板上的开口部分；半导体层，形成在绝缘基板的表面上，与像素电极间隔开，具有形成在其两个端部的源区和漏区，a除了像素电极的开口部分之外在绝缘基板的表面上形成的第一绝缘层，在半导体层上方的第一绝缘层上形成的栅电极，以及在除了开口之外的绝缘基板的表面上形成的第二绝缘层像素电极的一部分。本发明提供一种用减少的掩模工艺制造的有机EL显示器，其具有优异的电特性和改善的透光率。